IN THE CLAIMS

Please cancel Claims 1, 2, 10, 47, 48, 55, and 56 without prejudice or disclaimer.

Claims 1 and 2 (cancelled).

Claim 3 (currently amended): A method of converting a sample of an analog signal to a N-bit digital code, said method being performed in an analog to digital converter (ADC), said method comprising:

receiving said sample of said analog signal;

resolving P most significant bits (MSBs) of said N-bit digital code from said sample using one of a first reference voltage and a second reference voltage, wherein P is less than N; and

resolving Q bits of said N-bit digital code while using said first reference voltage to generate an equivalent voltage corresponding to said P MSBs and using said second reference voltage to generate an equivalent voltage corresponding to said Q bits,

wherein said Q bits form the next MSBs following said P MSBs,

~~The method of claim 2,~~ further comprising resolving next R bits of said N-bit digital code while using said first reference voltage to generate an equivalent voltage corresponding to both of said P MSBs and said Q bits, and said second reference voltage to generate an equivalent voltage corresponding to said R bits.

Claim 4 (currently amended): A method of converting a sample of an analog signal to a N-bit digital code, said method being performed in an analog to digital converter (ADC), said method comprising:

receiving said sample of said analog signal;

resolving P most significant bits (MSBs) of said N-bit digital code from said sample using one of a first reference voltage and a second reference voltage, wherein P is less than N; and

resolving Q bits of said N-bit digital code while using said first reference voltage to generate an equivalent voltage corresponding to said P MSBs and using said second reference voltage to generate an equivalent voltage corresponding to said Q bits,

wherein said Q bits form the next MSBs following said P MSBs.

~~The method of claim 2,~~ further comprises generating said first reference voltage using a first buffer and said second reference voltage using a second buffer.

Claim 5 (original): The method of claim 4, wherein the voltage level of said first reference voltage equals the voltage level of said second reference voltage.

Claim 6 (original): The method of claim 5, wherein said ADC comprises N capacitors operated according to successive approximation principle (SAP), wherein said N capacitors comprise P capacitors to resolve said P MSBs and Q capacitors to resolve said Q bits, wherein said resolving P MSBs comprises:

sampling said sample on said N capacitors in a sampling phase; and

connecting each of said P capacitors to said first reference voltage or ground based on a corresponding bit of said N_bit digital code in each iteration.

Claim 7 (original): The method of claim 6, wherein said resolving Q bits comprises connecting each of said Q capacitors to said second reference voltage or ground based on a corresponding bit of said N_bit digital code in each iteration, wherein each of said Q capacitors are connected to said first reference voltage or ground after

resolving said Q bits based on a corresponding bit of said N_bit digital code in each iteration.

Claim 8 (original): The method of claim 7, further comprises correcting an error in said P MSBs, said correcting comprises:

connecting a first capacitor to a ground before completing resolving of said P MSBs;

connecting a second capacitor to said first reference voltage before completing resolving of said P MSBs, wherein said first capacitor and said second capacitor are provided for said correcting; and

connecting said first capacitor to said first reference voltage if a voltage representing said P MSBs is less than a voltage level of said sample after resolving of said P MSBs, else connecting said second capacitor to ground.

Claim 9 (original): The method of claim 8, further comprises correcting an error in said Q bits, wherein said correcting said error in said Q bits comprises:

connecting a third capacitor to a ground before completing resolving of said Q bits;

connecting a fourth capacitor to said second reference voltage before completing resolving of said Q bits, wherein said third capacitor and said fourth capacitor are provided for said correcting said error in said Q bits; and

connecting said third capacitor to said first reference voltage if a voltage representing said P MSBs and said Q bits is less than said voltage level of said sample after resolving of said Q bits, else connecting said fourth capacitor to ground.

Claim 10 (cancelled).

Claim 11 (currently amended): A method of converting a sample of an analog signal to a N-bit digital code, said method being performed in an analog to digital converter (ADC), said method comprising:

receiving said sample;

resolving at least one most significant bits (MSB) of said N-bit digital code using a first DAC;

setting an intermediate digital value to equal said at least one MSB in corresponding bit positions; and

resolving at least one of the remaining bits of said MSB using a second DAC starting from said intermediate digital value,

~~The method of claim 10,~~ wherein each of said at least one MSB and at least one of the remaining bits are resolved according to a successive approximation principle (SAP).

Claim 12 (original): The method of claim 11, wherein said at least one MSB comprise M most significant bits (MSBs) of said N-bit digital code, wherein said at least one of the remaining bits comprise remaining (N-M bits) of said N-bit digital code.

Claim 13 (original): The method of claim 12, wherein said first DAC is implemented with a higher speed compared to said second DAC, and said second DAC is implemented with a higher SNR compared to said first DAC such that said ADC is provided with high speed and high SNR.

Claim 14 (original): The method of claim 13, wherein said first DAC comprises a first plurality of capacitors and said second DAC comprises a second plurality of capacitors, wherein a capacitance value of each of said second plurality of capacitors is greater than the capacitance value of a corresponding one of said first plurality of capacitors.

Claim 15 (original): The method of claim 14, further comprises:

providing a first reference voltage and a second reference voltage to said second DAC, wherein said first reference voltage and said second reference voltage are generated by a first buffer and a second buffer respectively.

Claim 16 (original): A successive approximation type analog to digital converter (SAR ADC) converting a sample of an input analog signal into an N-bit digital code, said SAR ADC comprising:

a SAR logic determining said N-bit digital code, said SAR logic providing an intermediate digital value in each iteration according to a comparison result which is based on a comparison of a voltage level equivalent of the intermediate digital value provided in a prior iteration with said sample;

a comparator providing said comparison result; and

a digital to analog converter (DAC) converting said intermediate value to an equivalent voltage level, said DAC receiving a first reference voltage and a second reference voltage, wherein said DAC generates said voltage level using said first reference voltage for a first subset of bits and said second reference voltage for a second subset of bits, wherein said first subset of bits and said second subset of bits are contained in said intermediate digital value.

Claim 17 (original): The SAR ADC of claim 16, wherein said voltage level represents a sum of a first voltage portion and a second voltage portion, wherein said first voltage portion represents an equivalent voltage corresponding to said first subset of bits and said second voltage portion represents an equivalent voltage corresponding to said second subset of bits.

Claim 18 (original): The SAR ADC of claim 17, wherein said first subset of bits comprise P most significant bits (MSBs) resolved in prior iterations, and said second subset of bits comprise Q bits following said P MSBs, wherein said Q bits are presently being resolved by said SAR ADC.

Claim 19 (original): The SAR ADC of claim 18, wherein an equivalent voltage corresponding to both of said P MSBs and said Q bits is generated using said first reference voltage in a subsequent iteration.

Claim 20 (original): The SAR ADC of claim 19, further comprising a first reference buffer providing said first reference voltage and a second reference buffer providing said second reference voltage.

Claim 21 (original): The SAR ADC of claim 19, wherein said DAC receives said sample and generates (a second input voltage - voltage of said sample + equivalent voltage of said intermediate digital value) as an input to said comparator, wherein '-' represents a subtraction operation and said second input voltage is also provided as an input to said comparator.

Claim 22 (original): The SAR ADC of claim 19, wherein said DAC generates an equivalent voltage corresponding to a next R bits of said N-bit digital code using said second reference voltage.

Claim 23 (original): The SAR ADC of claim 22, wherein the voltage level of said first reference voltage equals the voltage level of said second reference voltage.

Claim 24 (original): The SAR ADC of claim 22, wherein said DAC comprises N capacitors, wherein said N capacitors comprise P capacitors to resolve said P MSBs and Q capacitors to resolve said Q bits, wherein said N capacitors are connected to said sample in a sampling phase, and wherein each of said Q capacitors is connected to said second reference voltage or ground based on a corresponding bit of said N_bit digital code in said present iteration and to said first reference voltage or ground based on a corresponding bit of said N-bit digital code in said subsequent iteration.

Claim 25 (original): The SAR ADC of claim 24, further comprises a correction circuit correcting an error in said P MSBs, said correction circuit comprises:

a first capacitor connected to a ground before completing resolving of said P MSBs; and

a second capacitor connected to said first reference voltage before completing resolving of said P MSBs,

wherein said first capacitor is connected to said first reference voltage if a voltage representing said P MSBs is less than a voltage level of said sample after resolving of said P MSBs, else said second capacitor is connected to ground.

Claim 26 (original): A successive approximation type analog to digital converter (SAR ADC) converting a sample of an input analog signal into an N-bit digital code, said SAR ADC comprising:

a first digital to analog converter (DAC) converting a first input to an equivalent voltage level;

a second digital to analog converter (DAC) converting a second input to an equivalent voltage level wherein said second input comprises N-bits; and

a SAR logic sending a first sequence of input bit sets as said first input and determining a corresponding number of most significant bit (MSB) values, wherein each of said first sequence of input bit sets contains a number of bits equaling a number of bits in said first input, said SAR logic setting corresponding MSB positions of an intermediate digital value to the determined MSB values and sending said intermediate digital value as said second input to determine another bit of said N-bit digital code.

Claim 27 (original): The SAR ADC of claim 26, further comprising

a first comparator providing a first comparison result which is based on a comparison of said equivalent voltage of said first input with said sample;

a second comparator providing a second comparison result which is based on a comparison of said equivalent voltage of said second input with said sample; and

a multiplexor sending providing said first comparison result as an output when said SAR logic sends said first sequence of input bit sets as said first input, and said second comparison result as said output when said SAR logic sends said intermediate digital value as said second input, wherein said SAR logic determines each bit of said N-bit digital code according to said output.

Claim 28 (original): The SAR ADC of claim 26, wherein said first DAC is implemented with a higher speed compared to said second DAC, and said second DAC is implemented with a higher SNR compared to said first DAC such that said ADC is provided with high speed and high SNR.

Claim 29 (original): The SAR ADC of claim 28, wherein said first DAC comprises a first plurality of capacitors and said second DAC comprises a second plurality of capacitors, wherein a capacitance value of each of said second plurality of capacitors is greater than the capacitance value of a corresponding one of said first plurality of capacitors.

Claim 30 (original): The SAR ADC of claim 29, further comprises:

a first buffer and a second buffer, wherein said first buffer and said second buffer respectively provides a first reference voltage and a second reference voltage to said second DAC.

Claim 31 (original): A system comprising:

an analog processor processing an analog signal to generate a sample of an analog signal;

a successive approximation digital to analog converter (SAR ADC) converting said sample into an N-bit digital code, said SAR ADC comprising:

a SAR logic determining said N-bit digital code, said SAR logic providing an intermediate digital value in each iteration according to a comparison result which is based on a comparison of a voltage level equivalent of the intermediate digital value provided in a prior iteration with said sample;

a comparator providing said comparison result; and

a digital to analog converter (DAC) converting said intermediate value to an equivalent voltage level, said DAC receiving a first reference voltage and a second reference voltage, wherein said DAC generates said voltage level using said first reference voltage for a first subset of bits and said second reference voltage for a second subset of bits, wherein said first subset of bits and said second subset of bits are contained in said intermediate digital value.

Claim 32 (original): The system of claim 31, wherein said voltage level represents a sum of a first voltage portion and a second voltage portion, wherein said first voltage portion represents an equivalent voltage corresponding to said first subset of bits and said second voltage portion represents an equivalent voltage corresponding to said second subset of bits.

Claim 33 (original): The system of claim 32, wherein said first subset of bits comprise P most significant bits (MSBs) resolved in prior iterations, and said second subset of bits comprise Q bits following said P MSBs, wherein said Q bits are presently being resolved by said SAR ADC.

Claim 34 (original): The system of claim 33, wherein an equivalent voltage corresponding to both of said P MSBs and said Q bits is generated using said first reference voltage in a subsequent iteration.

Claim 35 (original): The system of claim 33, further comprising a first reference buffer providing said first reference voltage and a second reference buffer providing said second reference voltage.

Claim 36 (original): The system of claim 33, wherein said DAC receives said sample and generates (a second input voltage - voltage of said sample + equivalent voltage of said intermediate digital value) as an input to said comparator, wherein '-' represents a subtraction operation and said second input voltage is also provided as an input to said comparator.

Claim 37 (original): The system of claim 33, wherein said DAC generates an equivalent voltage corresponding to a next R bits of said N-bit digital code using said second reference voltage.

Claim 38 (original): The system of claim 37, wherein the voltage level of said first reference voltage equals the voltage level of said second reference voltage.

Claim 39 (original): The system of claim 38, wherein said DAC comprises N capacitors, wherein said N capacitors comprise P capacitors to resolve said P MSBs and Q capacitors to resolve said Q bits, wherein said N capacitors are connected to said sample in a sampling phase, and wherein each of said Q capacitors is connected to said second reference voltage or ground based on a corresponding bit of said N_bit digital code in said present iteration and to said first reference voltage or ground based on a corresponding bit of said N-bit digital code in said subsequent iteration.

Claim 40 (original): The system of claim 39, further comprises a correction circuit correcting an error in said P MSBs, said correction circuit comprises:

a first capacitor connected to a ground before completing resolving of said P MSBs; and

a second capacitor connected to said first reference voltage before completing resolving of said P MSBs,

wherein said first capacitor is connected to said first reference voltage if a voltage representing said P MSBs is less than a voltage level of said sample after resolving of said P MSBs, else said second capacitor is connected to ground.

Claim 41 (original): The system of claim 40, wherein said system comprises a global positioning system receiver, said system further comprising an antenna to receive said analog signal and provide said analog signal to said analog processor.

Claim 42 (original): A system comprising:

an analog processor processing an analog signal to generate a sample of an analog signal;

a successive approximation type analog to digital converter (SAR ADC) converting said sample into an N-bit digital code, said SAR ADC comprising:

a first comparator providing a comparison result of a first analog signal and said sample;

a second comparator providing a comparison result of a second analog signal and said sample;

a first digital to analog converter (DAC) receiving said sample and an intermediate P-bit digital value, said first DAC generating said first analog signal based on said intermediate P-bit digital value in each iteration;

a second DAC receiving said sample and an intermediate N-bit digital value, said second DAC generating said second analog signal based on said intermediate N-bit digital value in each iteration; and

a SAR logic determining said N-bit digital code by resolving a first subset of bits by interfacing with said first DAC and said first comparator, and then resolving a second subset of bits by interfacing with said second DAC and said second comparator, wherein said first subset of bits and said second subset of bits are used to generate said N-bit digital code.

Claim 43 (original): The system of claim 42, wherein said first subset of bits comprise M most significant bits (MSBs) of said N-bit digital code, wherein said second subset comprises remaining (N-M bits) of said N-bit digital code.

Claim 44 (original): The system of claim 43, wherein said first DAC is implemented with a higher speed compared to said second DAC, and said second DAC is implemented with a higher SNR compared to said first DAC such that said ADC is provided with high speed and high SNR.

Claim 45 (original): The system of claim 44, wherein said first DAC comprises a first plurality of capacitors and said second DAC comprises a second plurality of capacitors, wherein a capacitance value of each of said second plurality of capacitors is greater than the capacitance value of a corresponding one of said first plurality of capacitors.

Claim 46 (original): The system of claim 45, further comprises:

a first buffer and a second buffer, wherein said first buffer and said second buffer respectively provides a first reference voltage and a second reference voltage to said second DAC.

Claims 47 and 48 (cancelled).

Claim 49 (currently amended): An apparatus converting a sample of an analog signal to a N-bit digital code, said apparatus comprising:

means for receiving said sample of said analog signal;

means for resolving P most significant bits (MSBs) of said N-bit digital code from said sample using one of a first reference voltage and a second reference voltage, wherein P is less than N; and

means for resolving Q bits of said N-bit digital code while using said first reference voltage to generate an equivalent voltage corresponding to said P MSBs and using said second reference voltage to generate an equivalent voltage corresponding to said Q bits,

wherein said Q bits form the next MSBs following said P MSBs,

~~The apparatus of claim 48,~~ further comprises means for resolving next R bits of said N-bit digital code while using said first reference voltage to generate an equivalent voltage corresponding to both of said P MSBs and said Q bits, and said second reference voltage to generate an equivalent voltage corresponding to said R bits.

Claim 50 (original): The apparatus of claim 48, further comprises means for generating said first reference voltage using a first buffer and said second reference voltage using a second buffer.

Claim 51 (original): The apparatus of claim 50, wherein the voltage level of said first reference voltage equals the voltage level of said second reference voltage.

Claim 52 (original): The apparatus of claim 51, further comprises an analog to digital converter (ADC), wherein said ADC comprises N capacitors operated according to successive approximation principle (SAP), wherein said N capacitors comprise P capacitors to resolve said P MSBs and Q capacitors to resolve said Q bits, wherein said means for resolving P MSBs comprises:

means for sampling said sample on said N capacitors in a sampling phase; and

means for connecting each of said P capacitors to said first reference voltage or ground based on a corresponding bit of said N_bit digital code in each iteration.

Claim 53 (original): The apparatus of claim 52, wherein said resolving Q bits comprises means for connecting each of said Q capacitors to said second reference voltage or ground based on a corresponding bit of said N_bit digital code in each iteration, wherein each of said Q capacitors are connected to said first reference voltage or ground after resolving said Q bits based on a corresponding bit of said N_bit digital code in each iteration.

Claim 54 (original): The apparatus of claim 53, further comprises means for correcting an error in said P MSBs, said means for correcting comprises:

means for connecting a first capacitor to a ground before completing resolving of said P MSBs;

means for connecting a second capacitor to said first reference voltage before completing resolving of said P MSBs, wherein said first capacitor and said second capacitor are provided for said means for correcting; and

means for connecting said first capacitor to said first reference voltage if a voltage representing said P MSBs is less than a voltage level of said sample after resolving of said P MSBs, else means for connecting said second capacitor to ground.

Claims 55 and 56 (cancelled).

Claim 57 (currently amended): An apparatus converting a sample of an analog signal to a N-bit digital code, said apparatus comprising:

means for receiving said sample of a voltage level;

means for providing said sample of said voltage level as an input to a first digital to analog converter (DAC) to resolve a first subset of bits; and

means for providing said sample of said voltage level as an input to a second DAC to resolve a second subset of bits, wherein said first subset of bits and said second subset of bits are used to generate said N-bit digital code,

wherein said first subset of bits comprise M most significant bits (MSBs) of said N-bit digital code, wherein said second subset comprises remaining (N-M bits) of said N-bit digital code, and

~~The apparatus of claim 56,~~ wherein said first DAC is implemented with a higher speed compared to said second DAC, and said second DAC is implemented with a higher SNR compared to said first DAC such that said ADC is provided with high speed and high SNR.

Claim 58 (original): The apparatus of claim 57, wherein said first DAC comprises a first plurality of capacitors and said second DAC comprises a second plurality of capacitors, wherein a capacitance value of each of said second plurality of capacitors is greater than the capacitance value of a corresponding one of said first plurality of capacitors.

Claim 59 (original): The apparatus of claim 58, further comprises:

means for providing a first reference voltage and a second reference voltage to said second DAC, wherein said first reference voltage and said second reference voltage are generated by a first buffer and a second buffer respectively.